



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,497	02/01/2002	Kraig R. White	FIS920010178US1	4513
7590	06/28/2004		EXAMINER	
McGuireWoods LLP Suite 1800 1750 Tysons Boulevard McLean, VA 22102			TORRES, JOSEPH D	
		ART UNIT	PAPER NUMBER	
		2133	5	
DATE MAILED: 06/28/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. <u>10/066,497</u>	Applicant(s) <u>WHITE, KRAIG R.</u>
	Examiner <u>Joseph D. Torres</u>	Art Unit <u>2133</u>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 2/1/2002.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) 8 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 March 2002 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '44' in Figure 3. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 8 is objected to because of the following informalities: "perallocated" is not a word. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said refresh rate" in lines 12-14. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites, "said ECC memory allocation circuit stores perallocated addresses in said dynamic memory", which is incomprehensible (Note: addresses are used for accessing stored data, hence it is not clear what is meant by storing addresses in said dynamic memory).

Claims 2-9 depend from claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 7-11, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito; Yutaka et al. (US 6697992 B2, hereafter referred to as Ito).

35 U.S.C. 102(e) rejection of claims 1 and 10.

Ito teaches a memory system having a reduced refresh rate in a sleep mode (Figure 1 in Ito is a memory system and col. 12, lines 42-45 in Ito teach that in sleep mode refresh is executed in a long cycle of 10 seconds or more, i.e., a reduced rate: Note: Ito refers to sleep mode refresh as self refresh since self refresh mode is only available in reduced power or reduced standby mode, see col. 6, lines 38-40 in Ito), comprising: a dynamic memory (see Abstract in Ito); an error correction code (ECC) memory allocation circuit (ECC circuits 214A-214D in Figure 1 of Ito are error correction code (ECC) memory allocation circuits) for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode (col. 6, lines 38-40 in Ito teach that ECC circuits 214A-214D in Figure 1 are only used when memory goes into low speed operation or self-refresh mode: Note ECC parity for critical data must inherently be stored at non-critical addresses where no critical data is stored otherwise the ECC parity would be written over critical data, hence Ito teaches that ECC circuits 214A-214D in Figure 1 are identifying non-critical bit addresses in said dynamic memory that are not storing critical data and allocating said addresses as ECC addresses for use in storing ECC parity when entering from an active mode to self-refresh sleep mode); an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses (ECC circuits 214A-214D in Figure 1 of Ito are ECC encoders for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses); a refresh execution circuit for reducing said

refresh rate in said sleep mode and increasing said refresh rate in said active mode (Control Logic 209 in Figure 1 of Ito is a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode); and a ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode (ECC circuits 214A-214D in Figure 1 of Ito are codecs hence are also ECC decoders for decoding said critical bits encoded with said error correction codes when reentering said active mode; Note: col. 7, lines 35-45 in Ito teach that error correction is performed prior to returning to normal operation mode). Note: During normal mode ECC is not used hence all of the memory is available for data and all ECC parity used in sleep mode is discarded.

35 U.S.C. 102(e) rejection of claims 2 and 3.

Col. 14, lines 13-20 of Ito teach that a fuse storage device is used to set refresh cycle rates.

35 U.S.C. 102(e) rejection of claim 4, 5 and 11.

Ito teaches a storage device for storing a plurality of sleep mode refresh rate data (Col. 14, lines 13-20 of Ito teach that a plurality of fuse storage devices are used to set refresh cycle rates); and a temperature sensor (col. 7, lines 27-32, Ito), wherein said refresh execution circuit selects one of said sleep mode refresh rate data according to operating temperature (col. 11, lines 19-25, Ito also see claim 12 in Ito).

35 U.S.C. 102(e) rejection of claim 7.

Figure 12 in Ito teaches the use of Bose-Chaudhuri-Hocquenghem code.

35 U.S.C. 102(e) rejection of claims 8 and 13.

Col. 15, lines 31-67 in Ito teaches a parity area is preallocated for self refresh mode, hence a parity area is a preallocated memory area for storing ECC at preallocated addresses.

35 U.S.C. 102(e) rejection of claims 9 and 14.

See Figures 28-30 in Ito.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 6, 12 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito; Yutaka et al. (US 6697992 B2, hereafter referred to as Ito).

35 U.S.C. 103(a) rejection of claims 6 and 12.

Ito substantially teaches the claimed invention described in claims 1-5, 10, 11 (as rejected above).

However Ito does not explicitly teach that refresh rate is reduced by a 2X factor for each decade Celsius reduction in operating temperature.

The Examiner asserts that Figure 11 of Ito teaches that the retention rate of tailbits can be tracked at different retention rates. It would be an obvious engineering design choice to select ECC and refresh rate based on retention rates to optimize data throughput and error rate for a given device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ito by including an additional step of reducing refresh rate by a 2X factor for each decade Celsius reduction in operating temperature. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that reducing refresh rate by a 2X factor for each decade Celsius reduction in operating temperature would have provided the opportunity to optimize data throughput and error rate for a given device.

35 U.S.C. 103(a) rejection of claim 15.

Ito teaches a memory system having a reduced refresh rate in a sleep mode (Figure 1 in Ito is a memory system and col. 12, lines 42-45 in Ito teach that in sleep mode refresh is executed in a long cycle of 10 seconds or more, i.e., a reduced rate: Note: Ito refers to sleep mode refresh as self refresh since self refresh mode is only available in reduced power or reduced standby mode, see col. 6, lines 38-40 in Ito), comprising: a dynamic memory (see Abstract in Ito); an error correction code (ECC) memory allocation circuit (ECC circuits 214A-214D in Figure 1 of Ito are error correction code (ECC) memory allocation circuits) for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode (col. 6, lines 38-40 in Ito teach that ECC circuits 214A-214D in Figure 1 are only used when memory goes into low speed operation or self-refresh mode: Note ECC parity for critical data must inherently be stored at non-critical addresses where no critical data is stored otherwise the ECC parity would be written over critical data, hence Ito teaches that ECC circuits 214A-214D in Figure 1 are identifying non-critical bit addresses in said dynamic memory that are not storing critical data and allocating said addresses as ECC addresses for use in storing ECC parity when entering from an active mode to self-refresh sleep mode); an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses (ECC circuits 214A-214D in Figure 1 of Ito are ECC encoders for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses); a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode

(Control Logic 209 in Figure 1 of Ito is a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode); and a ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode (ECC circuits 214A-214D in Figure 1 of Ito are codecs hence are also ECC decoders for decoding said critical bits encoded with said error correction codes when reentering said active mode; Note: col. 7, lines 35-45 in Ito teach that error correction is performed prior to returning to normal operation mode).

Note: During normal mode ECC is not used hence all of the memory is available for data and all ECC parity used in sleep mode is discarded.

However Ito does not explicitly teach the specific use of a computer readable medium for storing instruction for implementing the design in Ito.

The Examiner asserts that use of a computer readable medium for storing instruction for implementing the design in Ito is an obvious Engineering design choice based on desired flexibility and scalability of the system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ito by including use of a computer readable medium for storing instruction for implementing the design in Ito. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a computer readable medium for storing instruction for implementing the design in Ito would have provided the opportunity to implement the design in Ito based on desired flexibility and scalability of the system.

35 U.S.C. 103(a) rejection of claim 16.

Ito substantially teaches the claimed invention described in claims 1-5, 10, 11 (as rejected above).

However Ito does not explicitly teach that refresh rate is reduced by a 2X factor for each decade Celsius reduction in operating temperature.

The Examiner asserts that Figure 11 of Ito teaches that the retention rate of tailbits can be tracked at different retention rates. It would be an obvious engineering design choice to select ECC and refresh rate based on retention rates to optimize data throughput and error rate for a given device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ito by including an additional step of reducing refresh rate by a 2X factor for each decade Celsius reduction in operating temperature. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that reducing refresh rate by a 2X factor for each decade Celsius reduction in operating temperature would have provided the opportunity to optimize data throughput and error rate for a given device.

35 U.S.C. 103(a) rejection of claim 17.

Col. 15, lines 31-67 in Ito teaches a parity area is preallocated for self refresh mode, hence a parity area is a preallocated memory area for storing ECC at preallocated addresses.

35 U.S.C. 103(a) rejection of claim 18.

See Figures 28-30 in Ito.

35 U.S.C. 103(a) rejection of claims 19 and 20.

Figure 12 in Ito teaches the use of Bose-Chaudhuri-Hocquenghem code. Note: Reed-Solomon code is a particular type of Bose-Chaudhuri-Hocquenghem code.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133